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RESEARCH ARTICLE

FPGA Based Signal Emulator for Radar Signal Processing

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ABSTRACT

This paper presents the design of signal simulator for advanced modern radar technology through field programmable gate array implementation. When considering all other possibilities, implementation of FPGA shows an impressive result in efficiency. By generating the complex waveform, chirp signal is sent to the destination by means of wide band spread spectrum. This approach is developed for an effective receiver end through filtering by using noise shaping, digital signal synthesizer and pulse accumulator. This system supports effective signal interference and jamming, and overcomes the inconvenience occur in its application.

Keywords: Radar technology, Field programmable gate array, Wide band spectrum, Signal interference, Filter.

1. INTRODUCTION

The advancement of modern electronically controlled weapons has created a major importance in the expansion of science and technology. It thus has evolved in modern Electronic Warfare (EW). EW can destroy the enemy battle by disabling their electronic equipment using electromagnetic emission through wide band electromagnetic spectrum. [1, 2] With the advent of rapid technology advances in converters and digital signal processing, digital receivers have been widely used in EW systems and are found to be effective. However, the testing and evaluation of the digital receiver based EW systems requires a big test set-up with a very high-end vector signal generator operated by sophisticated software for generating the various input signals such as Frequency Modulated (FM), Continuous Wave (CW), Frequency chirp, Agile and Linear FM.

[3] EW works on the basic usage of electromagnetic spectrum to control and attack the enemy fields. Through the usage of this advance move, opponents' actions are denied. EW can be applied from any place like space, landmass, water and air. Also, it is supportable for manned and unmanned operation and the communication of opponent can be completely destroyed. The advancement of EW is further divided into electronic support and electronic protection (counter and counter-counter measure). [4] Electronic support system supports to control the operation by which, we can able to detect and identify the disruption, intercept the signal, analyze and record the action of electromagnetic energy to identify and provide warning to the commanding operational person. It supports to produce the signal through electronic devices for intelligent communications without tracking the signal. It can also tap the military details of the enemy countries and record their operational concepts. This system works silently because of wide band spectrum, and higher range of power has been used to detect

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the signal pulses of the reflected signal. Due to better characteristic of this warfare system, the frequency of other countries cannot detect the unknown signal. Signal strength of the system is also unknown to the initial users. To transmit the signal, it requires 30MHz to 50GHz of the spectrum range.

[5] Electronic counter measure uses electrical or electronic components to track or to disturb the signal. It can able to trick the signals from sonar, radar and other components, and can be used to offense and defense the governing system. The counter measure concept has been used in aircraft to protect from attacks. It is also connected with advanced stealth equipment. Signals mostly get affected by means of jamming. Likewise the home missiles terminals are also get affected by jamming. Usually the electronic counter measure targets the radar by interfering with the signal, thus modifying the target. Interference occurs mostly by jamming, and high level echo signal is used to complicate the receiver. Transponders also increase the echo signal which transfers from small decoy devices to the larger range devices based on electromagnetic properties.

[6, 7] Electronic counter-counter measure gives an improved performance to minimize the effect of jamming and interference of the signal. This system is also said to be electronic protective measure, widely used to control the jamming signal. This electronic protection measure increases the signal strength and strengthens the sensors to receive more efficiently. It is used in aircraft that makes the system to ignore the signal. By chirping, the signal pulse gets compressed. Pulse compression method boosts the apparent signal strength. Carrier frequency varies in the pulse, which is reflected from the target and gets returned to the receiving end. At this time, the processing of the signal starts, thus leading to the addition of delay as a frequency function. Due to its stacking effect, the pulse would be stronger and has short duration such that the effect increases the strength of the received signal beyond noise jamming. The jamming pulse has different chirp and therefore any increase in signal strength would not have any effect on it. Frequency hopping switches the transmitted energy frequency at a rapid rate, and this frequency is received in the course of receiving time window. The foil jammer is unable to detect the frequency switch so easily and therefore it switches its jamming frequency at this window. This technique finds application in barrage jamming. By forcing the jammer to extend its strength through several frequencies in the jammed frequency range of the unit, it thus acts against barrage jamming. Such spread-spectrum methods avoid jamming of wide band signal by allowing the signals to get extended widely.

2. COMPLEX WAVEFORMS

Upstream and downstream of signal is varied by increasing and decreasing the frequency range. For sonar and radar, chirp is the signal that is used to transmit and receive the signal. Sometimes chirp signal is termed to interchange with sweep signal. Chirp signal has wide application areas such as spread spectrum. To demodulate, the chirp signaling devices has been used. In the field of optical communication, laser also exhibits same chirp signal due to the usage of propagation material [8-11]. Simple chirp waveforms are shown in figures 1 and 3.

Here to apply chirp signal, its frequency f(t) is varied with time.

$$f(t) = f_0 + k$$

where f_0 refers the carrier frequency (t=0) and k refers the frequency rate.

The function of normalized chirp signal corresponds to,

$$x(t) = \sin\left[2\pi\int_0^t f(t')dt'\right]$$

$$x(t) = \sin\left[2\pi\int_0^t (f_o + kt')dt'\right]$$

$$x(t) = \sin\left[2\pi\left(f_o + \frac{k}{2}t\right)dt'\right]$$

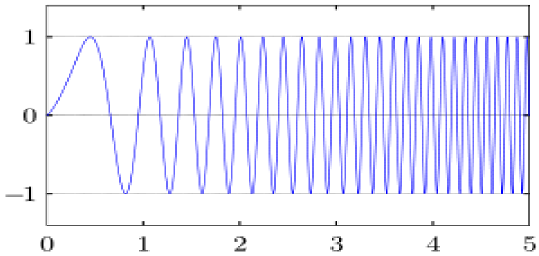

Figure 1.Waveform of linear chirp

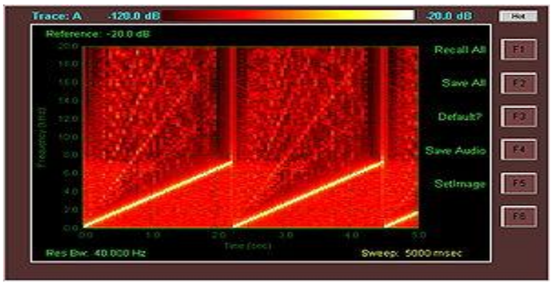

Figure 2.Spectrographic view of linear chirp waveform

Figure 2 explains about the spectrographic view of linear change by a time function. It is plotted by changing the frequency from 0 to 7kHz. The signal intensity is identified by frequency and time. Figure 4 shows the spectrographic view of simple chirp waveform.

In a form of exponential chirp, signal varies through frequency over time. Corresponding waveform is obtained by selecting two points at different time intervals t_1 and t_2. The ratio of frequency $f(t_2)/f(t_1)$ will be constant.

$$f(t) = f_0 + k^t$$

where f_0 is carrier frequency at time zero and k is an exponential frequency rate.

For a linear chirp, it has a constant chirp rate, but for the exponential chirp, it has an increasing chirp rate. The procedural time domain function is given as,

$$x(t) = \sin\left[2\pi \int_0^t f(t')dt'\right]$$

$$x(t) = \sin\left[2\pi f_0 \int_0^t k^{t'} dt'\right]$$

$$x(t) = \sin\left[2\pi f_0 \frac{k^t - 1}{\ln(k)} dt'\right]$$

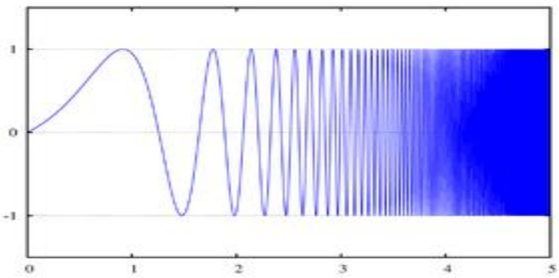

Figure 3.Simple chirp waveform

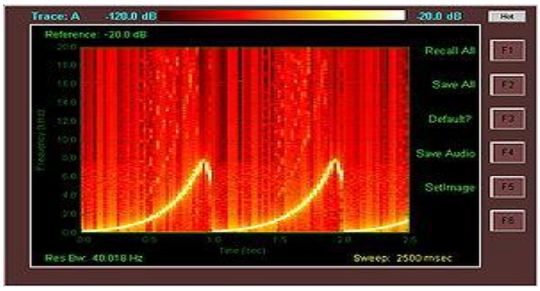

Figure 4.Spectrographic view of simple chirp waveform

Rate of changes in frequency of simple chirp waveform has been done by function of time. It is arranged by different cases; frequency is repeated from 0 to 8kHz every second. It can be seen through spectrographic view at 6kHz. In the process of linear chirp generation, normal exponential chirp has some basic frequency, $f(t)=f_0k^t$ added with harmonics. The correlation gain function does not have impact on generation process because of Doppler shift that scales up the wave frequency.

$$f(t)_{Doppler} = cf(t)_{Original}$$

where c is a constant.

From the above equation, increase of change in frequency correlates the original function that makes low reflection. In this same manner, Doppler shift works in geometric chirp wave formation which starts at various frequency range, f_0 that can be multiplied with constant c. If it is followed by exponential chirp after completion of original signal waves, it overlaps and starts the reflection. Due to this, correlation gain starts to improve. With an analog circuitry and linear or exponential ramping control voltage, chirp signal is generated. Also by changing the phase angle coefficient in sinusoid generating function, the signal has been generated digitally by a Digital to Analog Converter (DAC) and DSP. In the year 1954, Sidney Darlington patented the linear frequency modulation or the chirp modulation; later his work is continued by Winkler in 1962. These modulations would cause sinusoidal waveforms which in turn increases or decreases linearly, and such waveforms are generally called as chirps or linear chirps. The rates at which their frequencies get changes are termed as chirp rate. Here in binary chirp modulation, data transmission is achieved by mapping bits into chirps with respect to the opposite chirp rate.

Barker code sequence of N values ranges between +1 and -1, which is stated as,

$$\left|\sum_{J=1}^{N-v} a_j a_{j+v}\right| \leq 1 \text{ , for all } 1 \leq v < N,$$

where, j = 1, 2…

Barker code holds maximal autocorrelation sequence and has better RMS performance than any other codes. In spite of its low autocorrelation properties, it has been widely used in pulse compression radar systems and direct-sequence spread spectrum. The positive and negative amplitudes of the pulses make the Barker codes to use the biphase modulation. Also, it resembles a discrete version of continuous chirp. In wireless communications, sequences are chosen for their low cross correlation, and spectral properties are likely to be interfering with other sequences. 11 chip Barker sequences are used in 802.11b standard at speed rate 1-2Mbps and its autocorrelation functional value is 0 or ±1. It results with uniform spectrum and has good performance at the receiver side. Major components commonly used in the modern digital communication systems are Numerically Controlled Oscillators (NCO) or Direct Digital Synthesizers (DDS). In order to construct demodulators, up and down digital converters are used, and to implement different modulation schemes like PSK, FSK and MSK, quadrature synthesizers are used. A look-up table is used here to store the samples of digitally generated complex or real valued sinusoid, which is located in block or the distributed memory. Furthermore a digital integrator is used to generate a phase argument which is mapped by the look-up table to obtain the desired output waveform. Desired output frequency and spurs suppression of generated waveform are considered as the system level parameters and are accepted by simple user interface systems. The output frequency (f_{out}) of a synthesizer is given as follows:

$$f_{out} = f\left(f_{clk}, B_{\theta(n)}, \Delta\theta\right)$$

where f_{clk} is the system clock frequency, $B_{\theta(n)}$ is the number of bits used in phase accumulator and $\Delta\theta$ is the phase increment value. Δf, the frequency resolution of synthesizer is achieved by the combined function of clock frequency and $B_{\theta(n)}$. Phase increment ($\Delta\theta$) defines the output frequency of the synthesizer, which is an unsigned value.

In direct digital synthesizers, due to spectral purity consideration, the amplitude and phase quantization would affect the constancy of the signal formed from the look-up table by gathering the samples of sinusoid. Also the signal phase and amplitude resolution is affected with respect to the length and width of the look-up table. The limitations in resolutions are identical with time base jitter and amplitude quantization of a signal. The resolutions may add a white broad-band noise floor and spectral modulation lines to the signal spectrum. Frequency resolution is determined by the phase accumulator width [6], which coincides with the system clock frequency (f_{clk}). In real time application, it is necessary to allocate large number of bits to the accumulator to satisfy the system frequency resolution. A quantized version of phase angle is being used here due to its uncurbed memory requirement. In figure 1, Q1 block accomplishes the phase angle quantization. Quantizing the phase accumulator would result in the occurrence of jitter in output waveform; it could create an undesired phase modulation which is proportional to the quantization error.

Channels: Direct digital synthesizers core is able to generate single channel as well as multichannel implementation which could support up to 16 independent channels.

Direct digital synthesizers performance options: It would satisfy both the circuit and system-level performance requirements. The rate at which DSS core will be clocked is termed as DSS clock rate and the frequency domain requirements of out-of-band noise which is generated by DSS outputs are termed as Spurious Free Dynamic Range (SFDR). If the value of SFDR is 102dB or greater, then it forces to employ a Taylor series that results in implementation of the embedded multipliers.

Frequency resolution: It describes the granularity of tuning frequency. Let the value entered be 10 and then the tuning frequency is adjusted to 10Hz.

Noise Shaping: On the basis of several core factors including SFDR, the noise shaping type is attained automatically by selecting auto mode. On the other hand, selecting none leads to the production of a phase truncation DDS. When selecting phase dithering or Taylor Series Corrected (TSC), a dithered DDS or TSC DDS implementation is generated. TSC implementation supports only Virtex-II, Virtex-II Pro, Spartan-IIE, and Spartan-3 FPGAs. By correcting the radio signal using other architectural design, its connection switch is selected as off. So when the best method is selected, TSC is chosen. This series consists of 32 bit accumulator and 12 bit phase angle width. Read only memory block has been used for output to fix sine and cosine waveforms. Pipeline is also used here to increase the performance of core.

3. PROJECT FUNCTIONAL DESCRIPTION

For the implementation of radar design, the system requires input that is obtained from the antenna and interfaces with the FPGA kit virtex-4. The block and functional diagrams of FPGA implementation of signal simulator for radar systems is shown in figures 5 and 6 respectively. It consists of a simulator that consists of virtex-4 FPGA based hardware, high speed DAC, clock buffer and clock synthesizer.

DAC and clock synthesizer are initialized from Virtex-4 FPGA. 100MHz clock is generated from clock synthesizer LMX 2312 through SPI (Serial Peripheral Interface) protocol from Virtex-4 FPGA. The generated clock is buffered and fed to both FGPA and DAC. FPGA is configured in selected map mode generation of chirp and Barker signals.

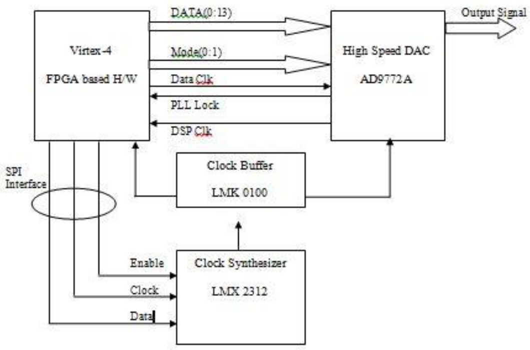

Figure 5.Block diagram of FPGA implementation of signal simulator for radar systems

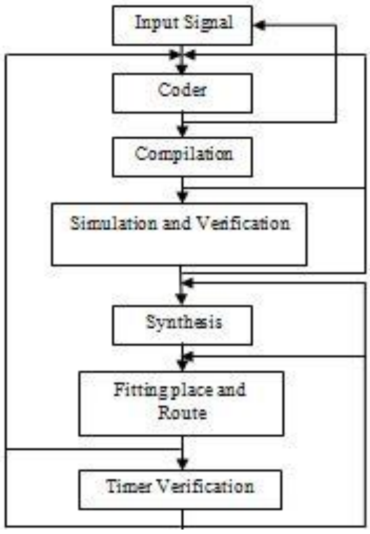

Figure 6 Functional diagram of FPGA implementation of signal simulator for radar systems

Complex waveforms are generated using IP core DDS in FPGA. Required frequency is thus generated, and based on our requirement, pulse width and pulse repetition frequencies are generated. The DDS data is varied between the minimum and maximum frequencies for the generation of chirp signal. For the generation of barker signal, the DDS offset is changed between 0° and 180° based on the barker bit length and type of modulation on the generated pulse width. This process is repeated at the rate of pulse repetition frequency. After applied modulation, the required digital data from FPGA is given to DAC. DAC generates the required modulated output signal. Usually analog input values are given by means of number sequence instead of impulses for a favorable sampling interval. Clock signal is used to latch and create a number of sequences. Due to this, DAC output varies from the previous obtained value. This obtained output value is represented by current number of latches. So the output voltage obtained from this effect shows the result of current values till the next sequences. From this resultant output, it shows staircase form of the output. The obtained resultant value is equivalent to the hold operation of zero order. Its impact gives a frequency response for reconstructed signal. DAC output gives a constant staircase value. It is said to be zero order hold operation. Sample rectangular number of sequences gives a triple level harmonics which is higher than Nyquist frequency and this effect is filtered by using low pass filter. Here low pass filter is used as a reconstruction filter.

4. RESULT AND DISCUSSION

With the implementation of waveform in FPGA hardware, the performance is improved. By the input signal, virtex-4 FPGA gives the parameter values through the simulation result. The output waveforms of DDS and DAC are shown in figures 7 and 8 respectively.

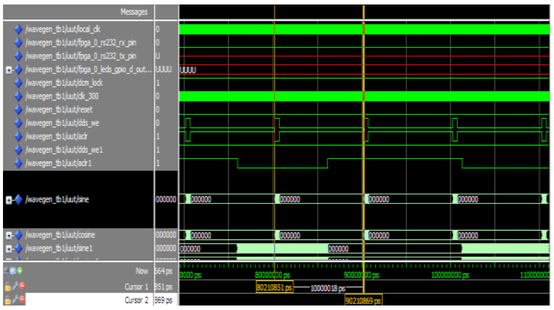

Figure 7.DDS implementation

For the generation of chirp and barker signal, frequencies are modulated through direct digital synthesizers. This process gets repeated on all the sequences, where several data may occur between frequencies. All the data are sequenced and modulated through FPGA hardware.

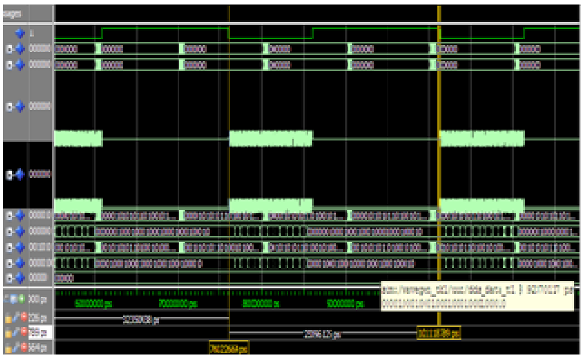

Figure 8.DAC waveforms

Analog inputs are given in terms of sequences and samples. Clock signals are used as latches. By doing this, barker sequences are generated as shown in figure 9.

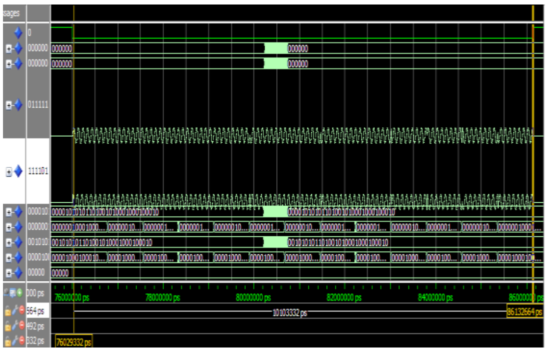

Figure 9.Barker sequence generation

Resultant values are increased by staircase form, and then the sequence values get filtered by using the low pass filters. Finally the desired chirp and barker waveforms are obtained as shown in figures 10 and 11.

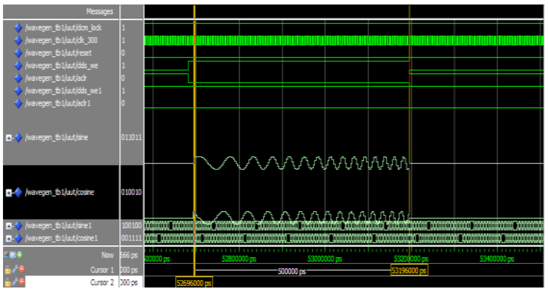

Figure 10.An exponential chirp waveform generator

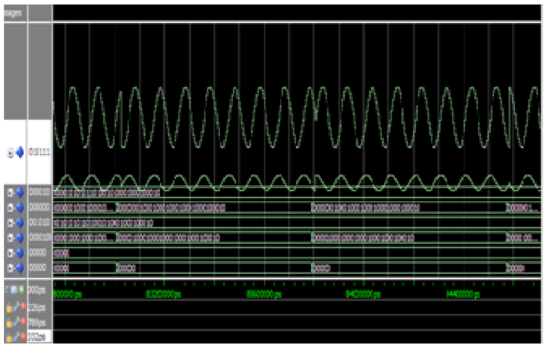

Figure 11.Barker Waveform Generation

5. CONCLUSION AND FUTURE SCOPE

In this paper, advanced radar technology has been developed by using FPGA implementation. Through this, it generates the complex waveforms like chirp and Barker code and the results are observed. The results are satisfactory and match with the required waveforms. These output waveforms can be fed to the electronic warfare system for its evaluation. This simulator is compact, cost effective and is implemented with FPGA and DAC. Due to the rapid technology advances of FPGA or DAC ICS, the current version of

ICs may go obsolete. However, the existing VHDL code can easily ported to higher version ICS to achieve the required function. Since the approach used is generic, it can be used as a baseline to generate different modulations required for the evaluation of EW systems or sub systems through combinations of both Barker and chirp signal.

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